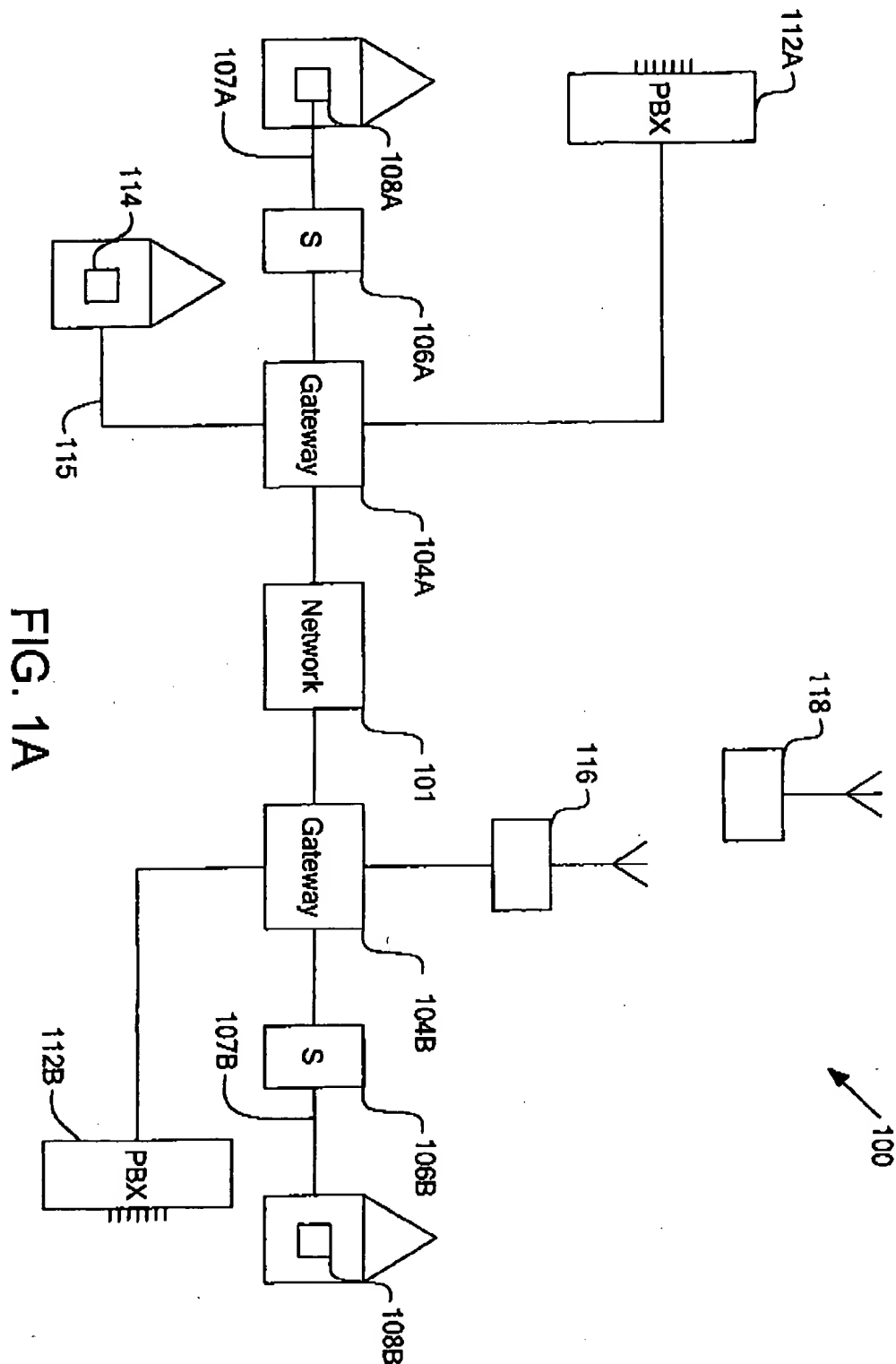


*Attorney Docket No.: 42.P12534*  
*Application No.: 09/938,104*  
*Page 2*

***IN THE DRAWINGS:***

Please replace the originally filed Figs. 1-18 with the replacement Figs. 1-18 filed  
herewith.

Replacement Sheet 09/938/04



Replacement Sheet 09/938 104

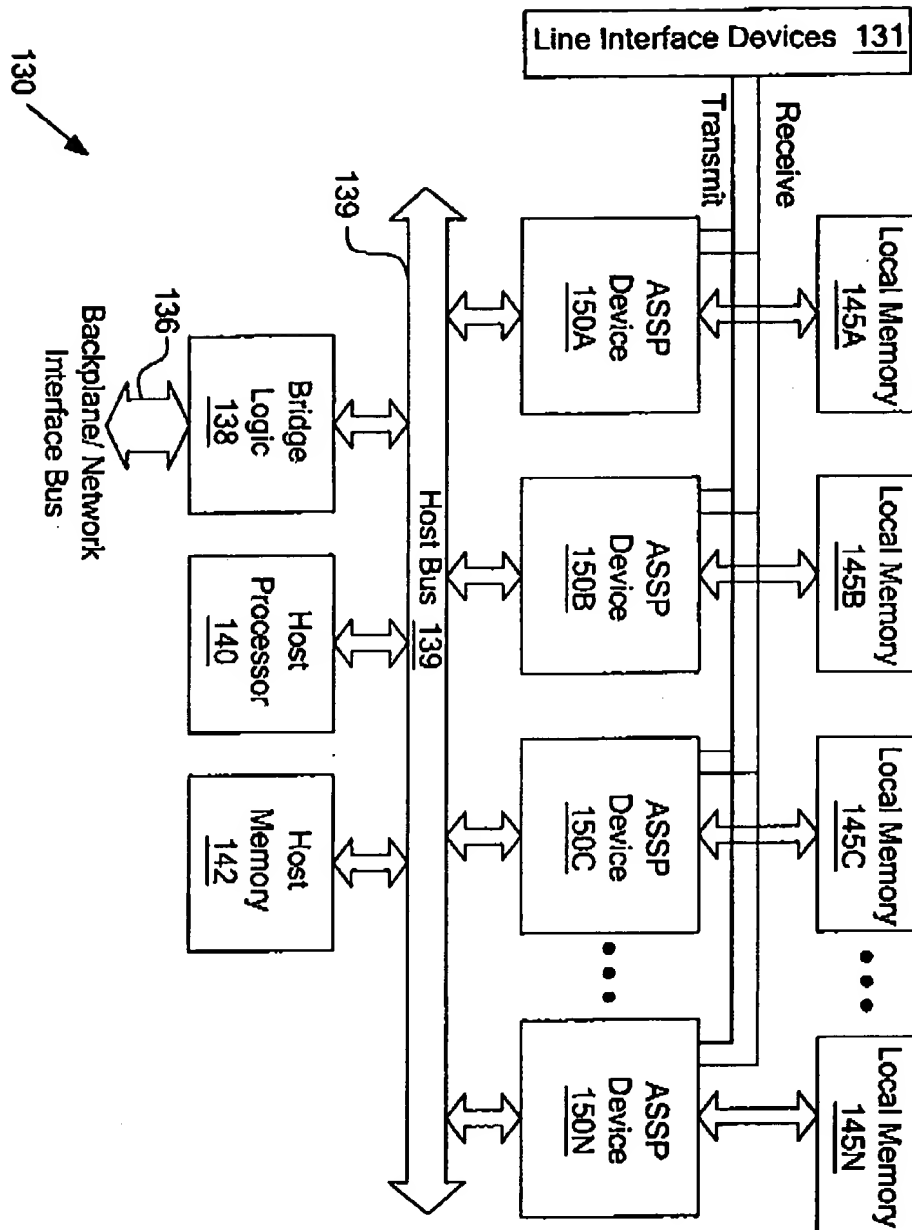


FIG. 1B

Replacement Sheet 09/938 104

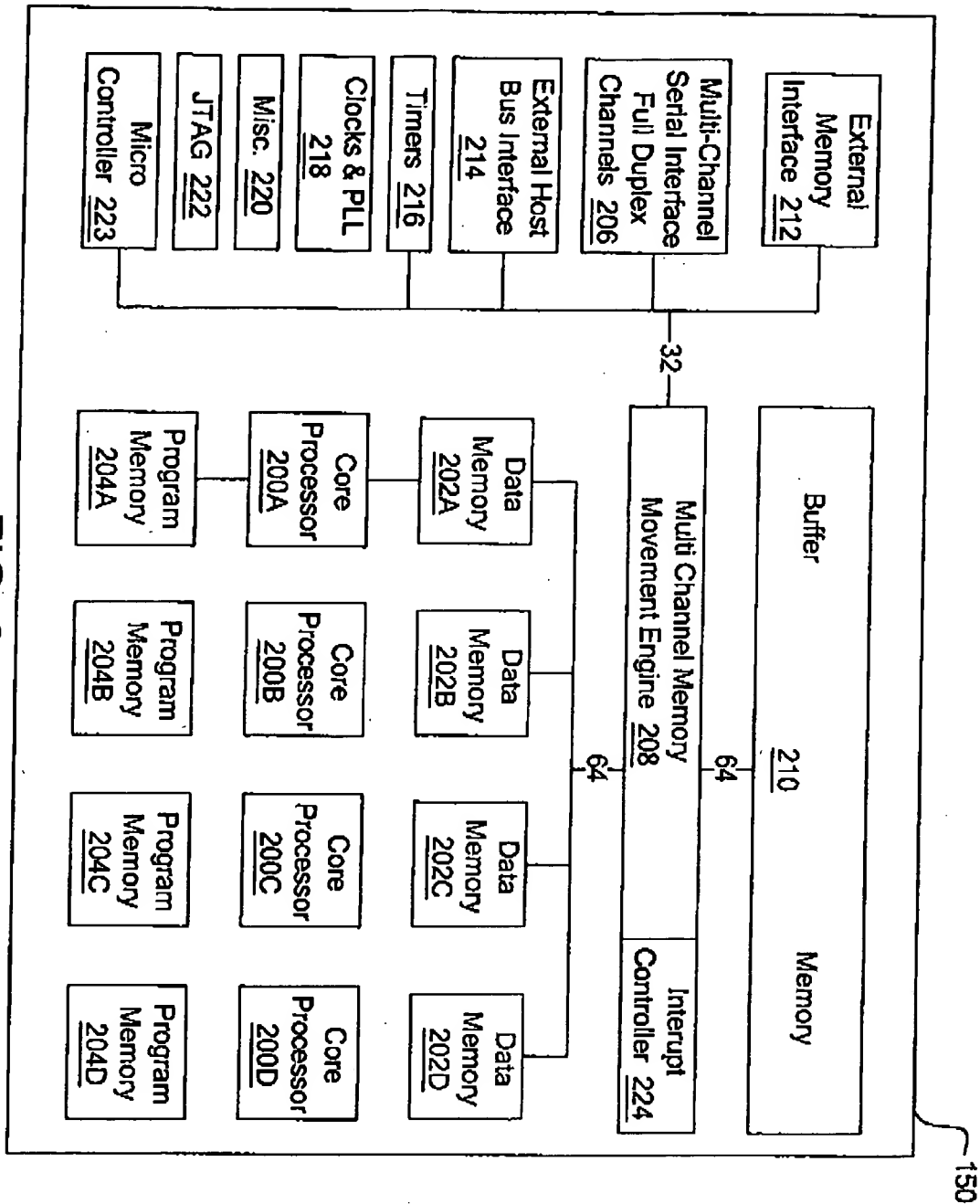


FIG. 2

Replacement Sheet 09/938104

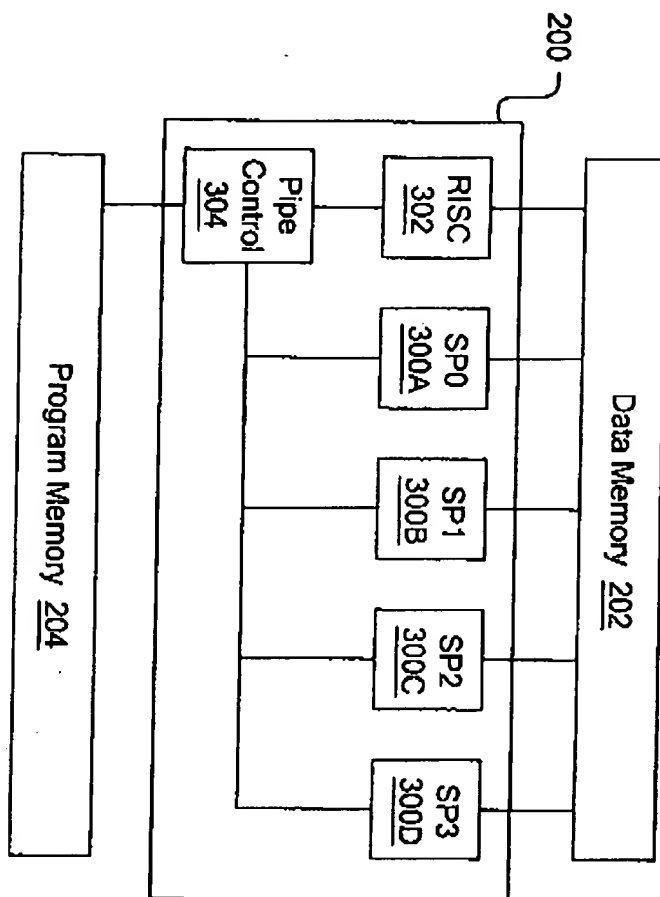


FIG. 3

Replacement Sheet 09/938104

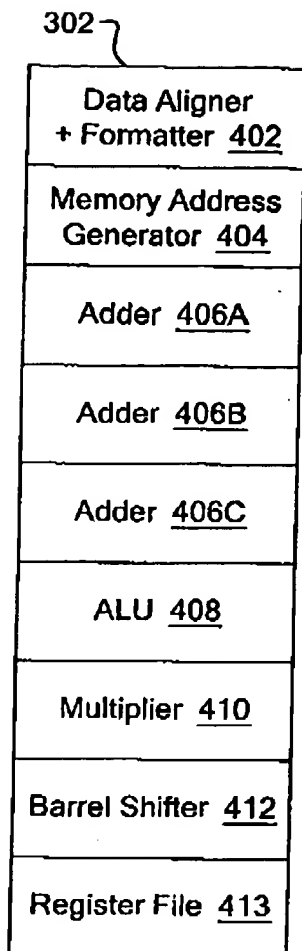


FIG. 4

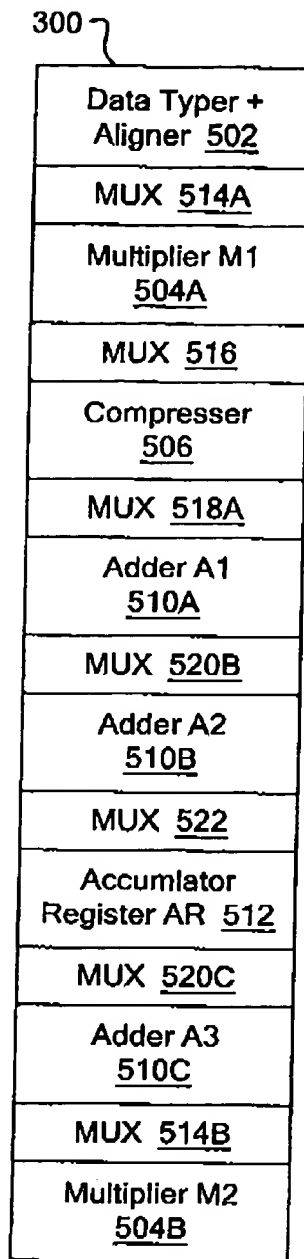


FIG. 5A

Replacement Sheet 09/938 104

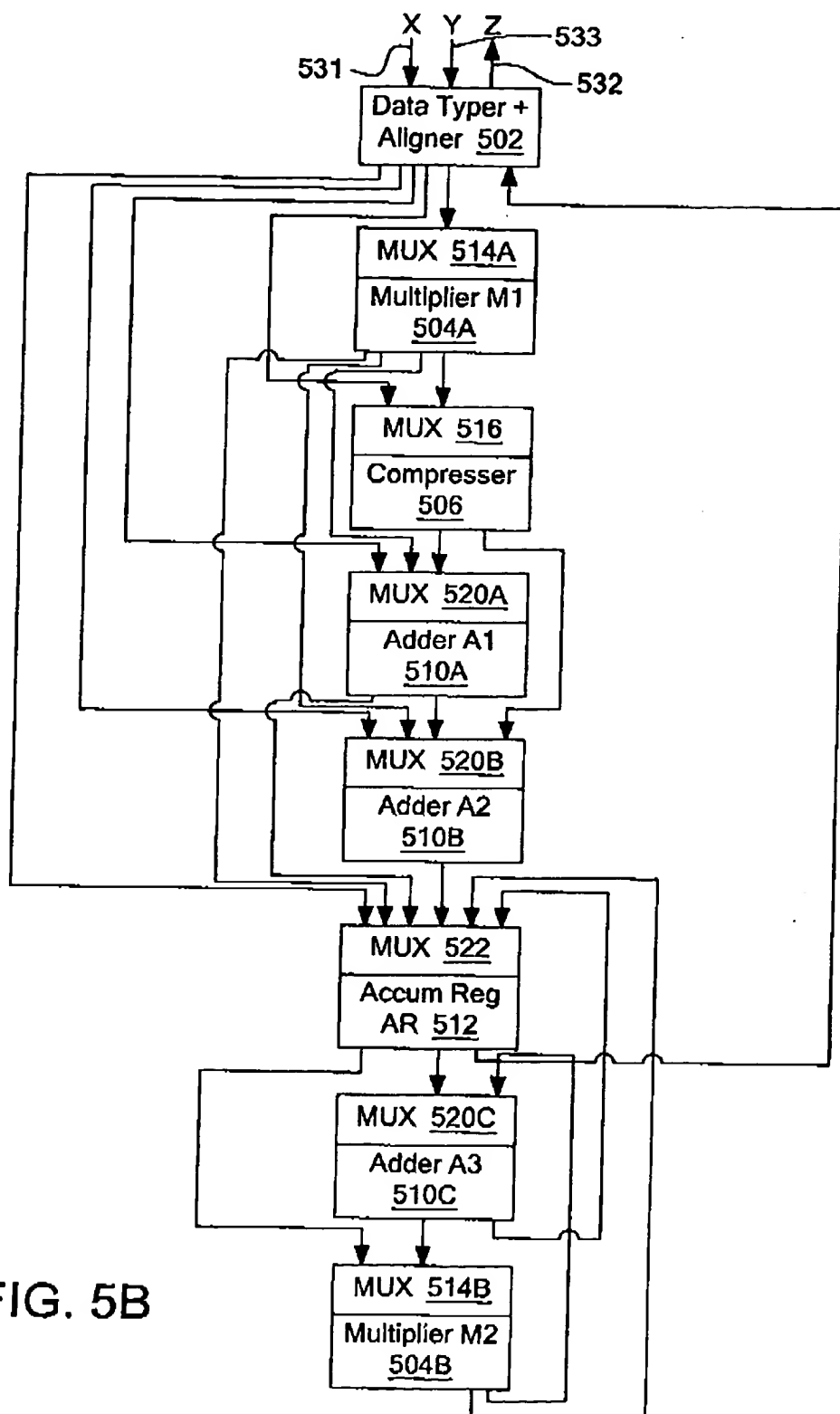


FIG. 5B

Replacement Sheet 09/938104

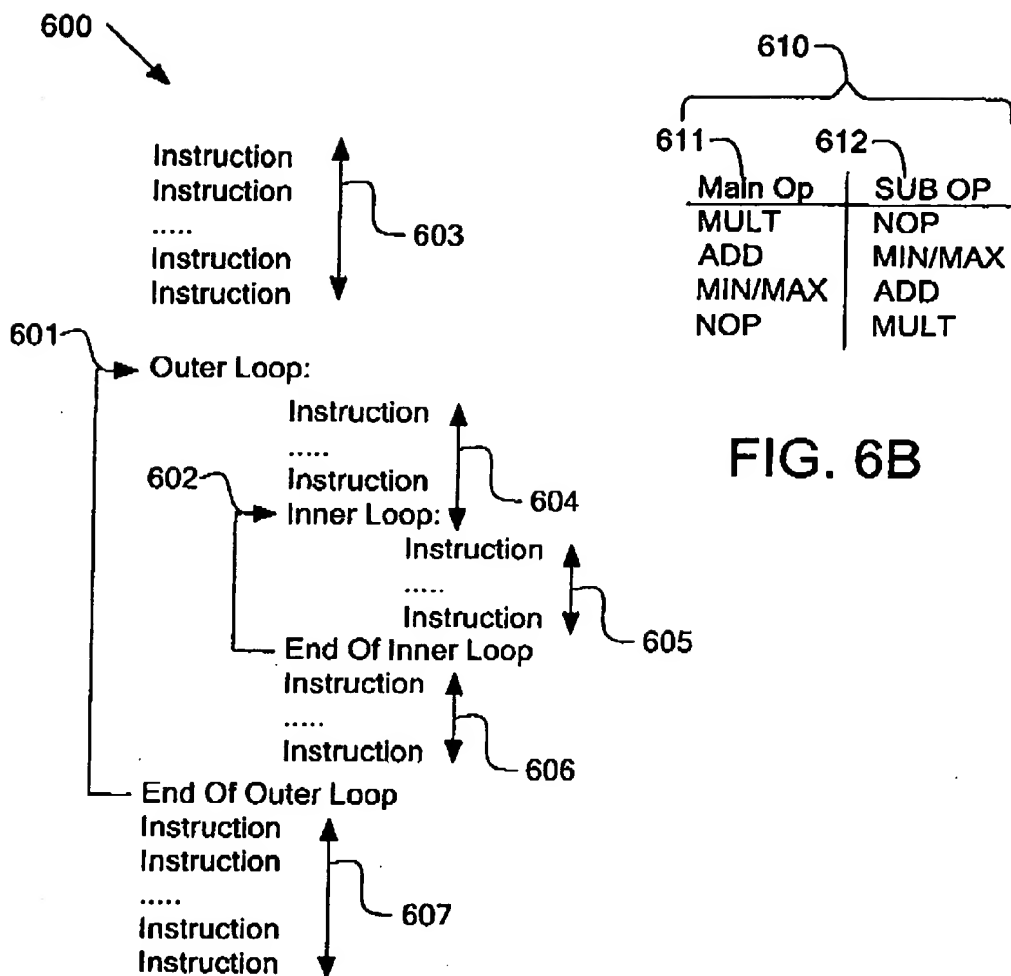


FIG. 6B

FIG. 6A



Replacement Sheet 09/938 104

20-bit ISA

39	18
0	0
0	1
1	0
1	1

 20-bit parallel  
 20-bit serial  
 40-bit extended  
 20-bit serial

 Control # Control  
 Control # Control  
 DSP, extensionsShadow  
 DSP # DSP

DSP Instructions

Multiply

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
1	0	0	0	PS	S*	SX					SY			V/S	SA	DA	0	0	0

 $da = sx * sy$   
 $da = (sx * sy) + ba$   
 $da = (sx * sa) + sy$   
 $da = (sx * sy) - sa$   
 $da = (sx * sa) - sy$   
 $da = min(sx * sy, sa)$   
 $da = min(sx * sa, sy)$   
 $da = max(sx * sy, sa)$ 

Add

1	0	1	PS	+/		SX					SY			V/S	SA	DA	0	0	0
---	---	---	----	----	--	----	--	--	--	--	----	--	--	-----	----	----	---	---	---

 $da = sx + sy$   
 $da = sx + sy + sa$   
 $da = sx + sy; sa = sx + sy;$   
 $da = (sx + sy) * sa$   
 $da = -(sx + sy) * sa$   
 $da = min(sx + sy, sa)$   
 $da = max(sx + sy, sa)$   
 $da = sum(sx, sy)$ 

Extremum

1	1	0	PS	X/N		SX					SY			V/S	SA	DA	0	0	0
---	---	---	----	-----	--	----	--	--	--	--	----	--	--	-----	----	----	---	---	---

 $da = ext(sx, sy)$   
 $da = ext(sx, sy, sa)$   
 $da = ext(sx, sa, sy)$   
 $da = -ext(sx, sa, sy)$   
 $da = ext(sx, sa) + sy$   
 $da = ext(sx, sa) - sy$   
 $ext(sa, da) ? 1 = sx, 0 = sy, ics = lc$ 

 type-match  
 Permuto  
 Reserved

1	1	0	PS	0		SX					SY			X	X	X	1	1	1
1	1	0	PS	1		SX					Type			X	ereg		1	1	1
1	1	1	PS	X		SX					SY			SA	DA	V/S			

 Nop  
 Add  
 AddSub  
 Mul  
 Min  
 Min  
 Min  
 Min  
 Max  
 Combadd  
 Nop  
 Ext  
 Min  
 Min  
 Add  
 Sub  
 emax  
 Permuto

FIG. 6E1

Replacement Sheet 09/938104

## Control and Specifier Extensions

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

0	Pred	PL	Sxt	Syt	Rnd	Lf	S'	S'	S'	0	SA	DA	abs	0	0
---	------	----	-----	-----	-----	----	----	----	----	---	----	----	-----	---	---

AddSub  
min/max

Add

0	Pred	PL	Sxt	Syt	Lf	Sub-ext	0	SA	DA	abs	0	0
						+/-	+/-	+/-	x			
						x	V/S	Rnd	Fp			
						lf-cl	Gx	Gx	Fp			

Nop  
Min/MaxIn  
Min/Max

Ext

0	Pred	PL	Sxt	Syt	Lf	Gx	Sub-ext	0	SA	DA	abs	0	0
						Lf	Fp						
						Rnd	V/S						

AddSub  
Mul

0	Pred	PL	Sxt	Pc11	0	ereg	Pc11	0	0
---	------	----	-----	------	---	------	------	---	---

## Type/offset/permute extensions

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

0	Pred	PL	X	Type: SX	Type: SY	0	SA	DA	x	0	1
0	Pred	PX	Psx	Permute: SX	Permute: SY	0	SA	DA	PSY	1	0
0	Pred	LR	Prx	Offset: SX	Offset: SY	0	SA	DA	Prx	1	1

Type override  
Permute override  
Offset override

## Shadow DSP

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Op	PL	op	ereg	ereg	1	SA	DA	Sub-op										

FIG. 6E2

Replacement Sheet 09/938 104

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
addsub	L	Pred	0	0	0			RX				RY				RZ			+	0
max/min	L	Pred	0	0	0			RX				RY				RZ			X/N	1
Shift	L	Pred	0	0	0			RX				RY				RZ			U1	RL
Logic	L	Pred	0	1	0			RX				RY				RZ			&	&
Mux	L	Pred	0	1	1			RX				RY				RZ			Pd	0
mov	L	Pred	0	1	1			RX				RY				RZ			0	1
addl	L	Pred	0	1	1			S14				DX				RZ			0	1
mov2reg	L	Pred	0	1	1			RX				unit				RZ			0	1
Ldm	L	Pred	0	1	1			RX				unit				RZ			0	1
bits	L	Pred	0	1	1			RX				unit				RZ			0	1
bits	L	Pred	0	1	1			RX				unit				RZ			0	1
Setbit	L	Pred	1	0	0			U14:POS				RZ				RZ			0	1
Move	L	Pred	1	0	0			U14:POS				RZ				RZ			0	1
Jump	L	Pred	1	0	0			U14:POS				RZ				RZ			0	1
Call	L	Pred	1	0	0			U14:POS				RZ				RZ			0	1
Loop	L	Pred	1	0	1			S18				S19				PZ			0	1
Impl	L	Pred	1	0	1			S19				S19				PZ			0	1
Call	L	Pred	1	0	1			U15:count				U15:count				PZ			0	1
Loop	L	Pred	1	0	1			RX				U15:count				PZ			0	1
Test	L	Pred	1	0	1			RX				U15:count				PZ			0	1
Testbit	L	Pred	1	0	1			RX				U15:count				PZ			0	1
Andp,orp	L	Pred	1	1	0			RX				U15:count				PZ			0	1
Load	L	Pred	1	1	1			Pa				P5				PZ			0	1
Store	L	Pred	1	1	1			MX				RZ				PZ			0	1
Store	L	Pred	1	1	1			MX				RZ				PZ			0	1
Extended	L	Pred	1	1	1			MX				RZ				PZ			0	1
Logic2	L	Pred	1	1	1			MX				RZ				PZ			0	1
mov-reg	L	Pred	1	1	1			MX				RZ				PZ			0	1
Cro	L	Pred	1	1	1			unit				RY/RZ				PZ			0	1
Parity	L	Pred	1	1	1			RX				RZ				PZ			0	1
Slim	L	Pred	1	1	1			RX				RZ				PZ			0	1
Abs	L	Pred	1	1	1			MX				RZ				PZ			0	1
Neg	L	Pred	1	1	1			RX				RZ				PZ			0	1
Div-step	L	Pred	1	1	1			RX				RZ				PZ			0	1
Set	L	Pred	1	1	1			RX				RZ				PZ			0	1
Reserved	L	Pred	1	1	1			RX				RZ				PZ			0	1
Return	L	Pred	1	1	1			Pred				PZ				PZ			0	1
Zero-ac	L	Pred	1	1	1			ac#				PZ				PZ			0	1
esync	L	Pred	1	1	1			RZ				PZ				PZ			0	1
Swi	L	Pred	1	1	1			U13				PZ				PZ			0	1
Nop	L	Pred	1	1	1			U13				PZ				PZ			0	1

FIG. 6F

&lt;Bit1, Bits3-6&gt; == U15 (Shift Amount)

&lt;Bit3, Bits13-10&gt; == U15 POS

Replacement Sheet 09/938104

## Extended Control

### Insert/Extract

**Insert  
Shift**

## Results

**jmp, call**  
**o3bop**

**droopi**

15

Reserved  
loglcp

## Test

**loadi**

load  
stone!

**Addis**

**Abstract**

Bits 13:2 of upper half (32:20)												
13	12	11	10	9	8	7	6	5	4	3	2	19:18
RX								0	0	0	0	X
U4:Length												
RX								0	0	0	0	Rxn
RX								0	0	0	0	X
U4:outer LC								0	0	1	0	X
RX								0	0	1	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X
RX								0	1	0	0	X

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MAC:

[illegible]

MUL-NOP  
MUL-ADD  
MUL-EXT  
MUL-MUL

**ABSTRACT:**

[illegible]

**Ex:**

[illegible]

**Logic:**

Group	Pred	opposite										same																											
		SX					SY					DZ																											
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**SHIFT:**[illegible]Shift  
Insert/extract  
Setbits

**Immediate:**

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		opcode				D2				BX				D2						Subop				term32								limit5						RMOV	

**Subop  
MOY  
ADD  
SUB  
MIN  
MAX  
AND  
OR**

## Task

[illegible]

**Branch:**

[illegible]

**Misc:**

**FIG. 6H**

Replacement Sheet 09/938104

### 7-bit specifier: Parallel Store, Parallel Load in DSP Instructions

6	5	4	3	2	1	0
MAR						

```
MemDir || pr += kds
MemDir += ids
```

**plrp14, p15**

**Always postupdate  
Always preupdate**

0	0	0	SPR p0-p15
0	0	1	reserved
0	1	0	sc-names
0	1	1	ppr: r0-r15
0	1		pir (r0 to (r15))
1	1		pir s1 Uia
			pir

### 6-bit specifier: DSP Instructions

M/R	5	4	3	2	1	0
-----	---	---	---	---	---	---

**MLR**

0	0	sc-names
0	1	ppr: r0-r15
1	pr (r0)	lo (r15) pr

□

sc-names  
ppr: r0-r15  
to (r15)

**Always postupdate**

### 5-bit specifier: RISC instructions

4	3	2	1	0
---	---	---	---	---

0	spr: p0-p15
0	ppr: n0-r15

**4-bit specifier:**

3	2	1	0
---	---	---	---

pbr: r0-r15	
pbr (r0-7)	plr
ereg	

**AR**

**RISC Instructions**  
**20-bit DSP Instructions**  
**20-bit Shadow DSP Instructions**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
type						permute				C8		idx1 Ulp (0-7)		idx0: S16 (-10 to 15)																	
																								p1r							

**FIG. 611**

Replacement Sheet 09/938/04

	ppr-type	
	ereg-type	
	hj-bl	
	pis-pir	
	cb-clr	
	loop-cr	
	pcl	
	status	
sc-names:		
A0	(use type, SIMD)	
A1		
T		
TR		
A00 (unit 0)		
A10		
T0		
TR0		
SX1		
SX1s		
SX2		
SX2s		
SY1		
SY1s		
SY2		
SY2s		
ereg-names:		
A0		
A1		
T		
TR		
PP0		
Asul		
PPl		
Deut		
SX1		
SX1s		
SX2		
SX2s		
SY1		
SY1s		
SY2		
SY2s		

**FIG. 612**

Replacement Sheet 09/938104

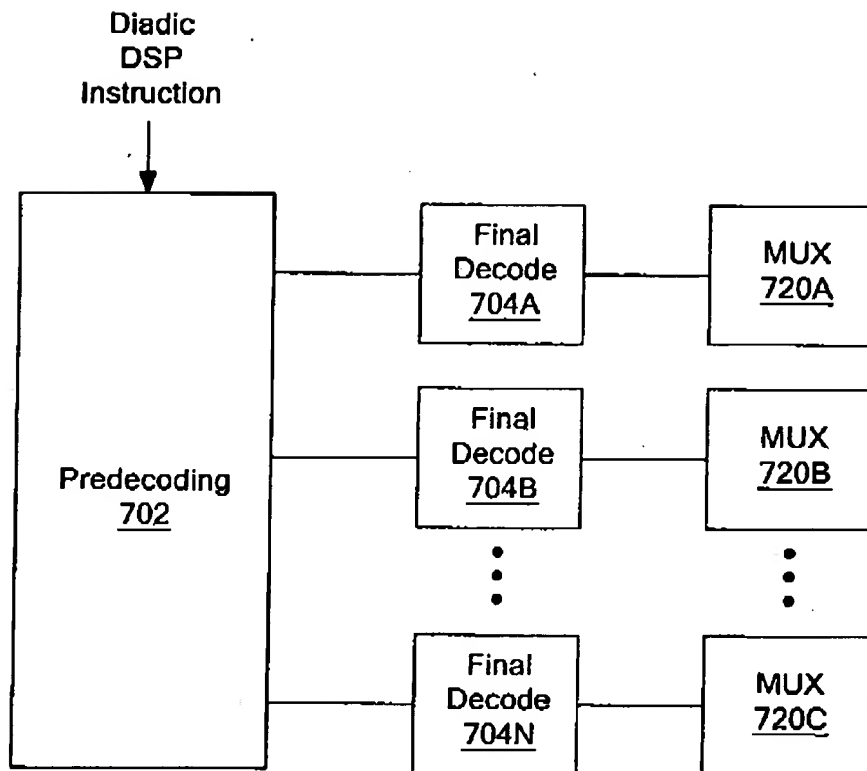
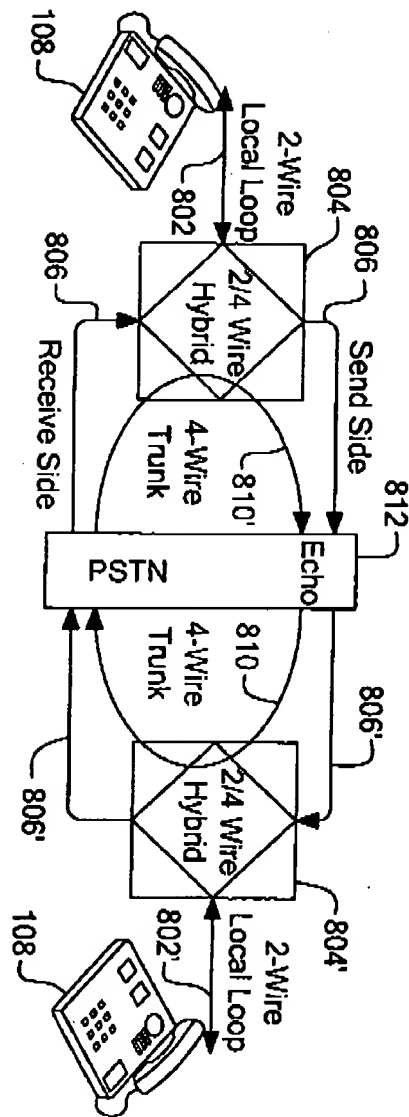


FIG. 7

Replacement Sheet 09/938 104



**FIG. 8**  
(Prior Art)

Replacement Sheet 09/938104

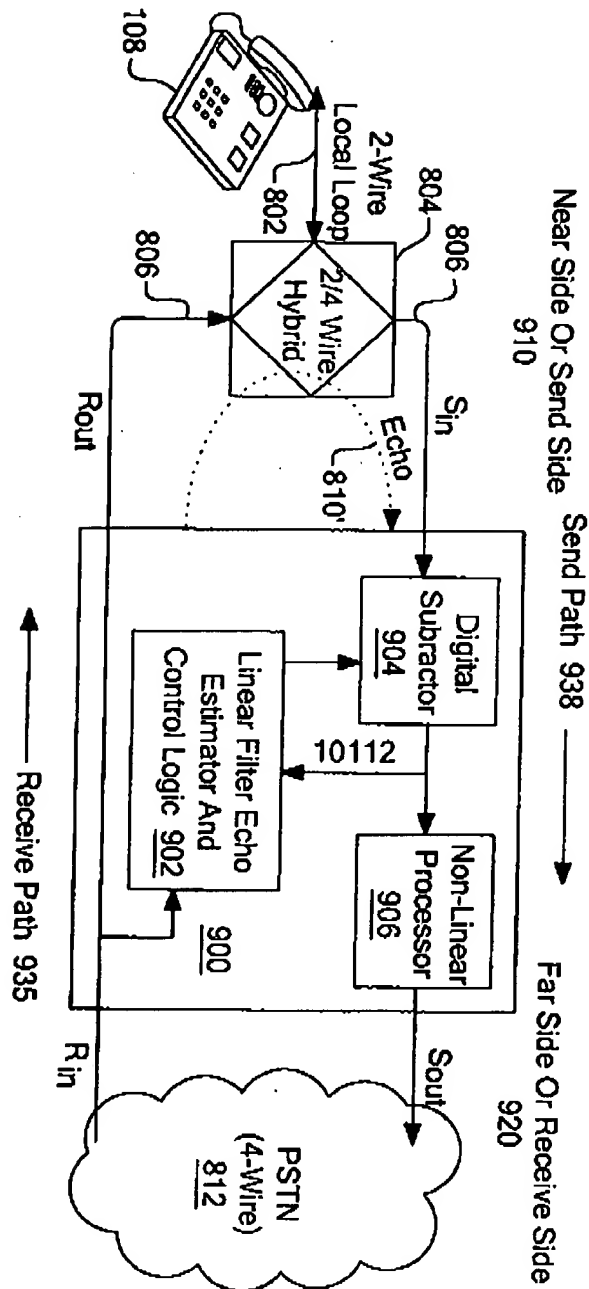
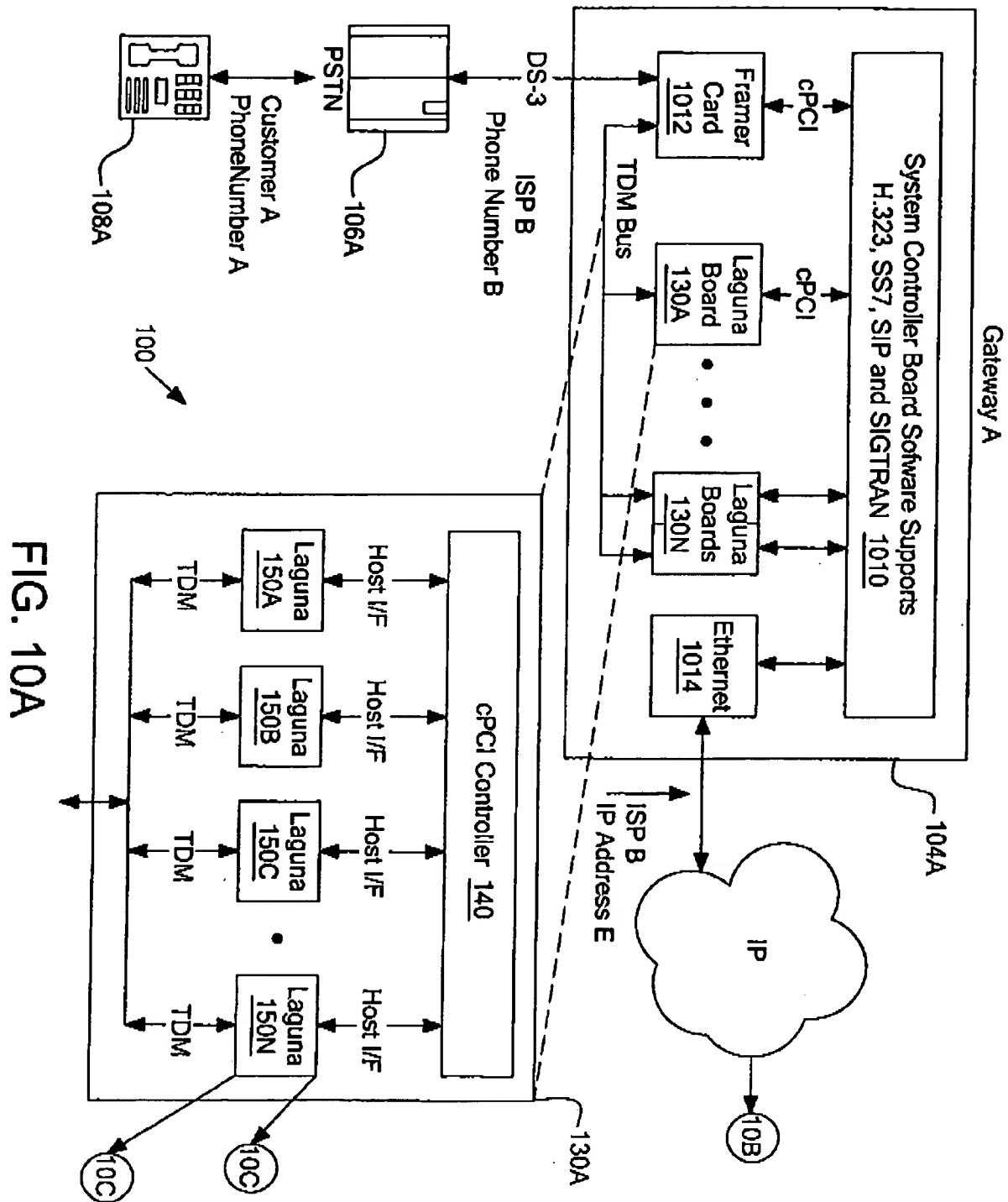


FIG. 9  
(Prior Art)

Replacement Sheet 09/938104



Replacement Sheet 09/938104

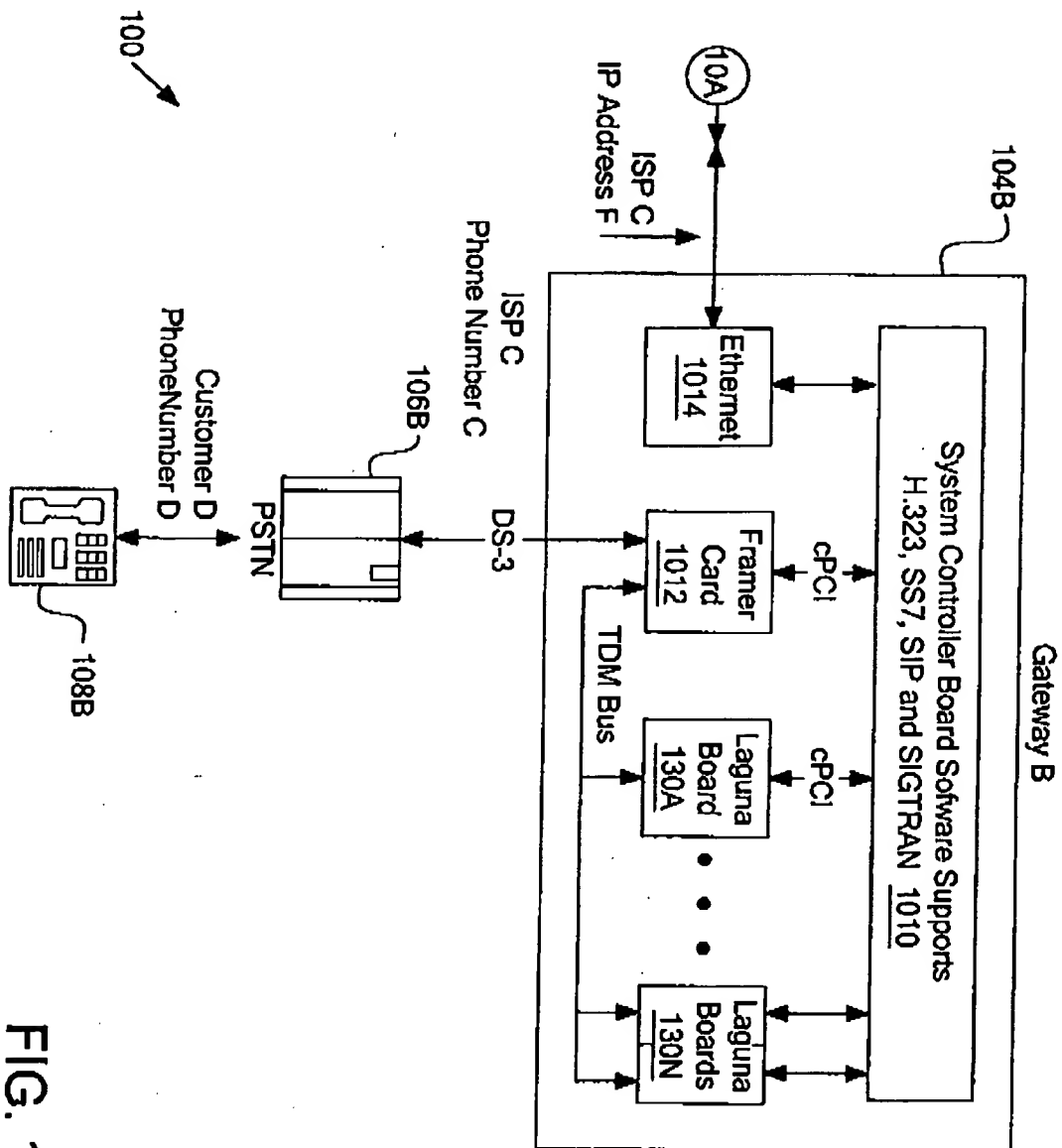
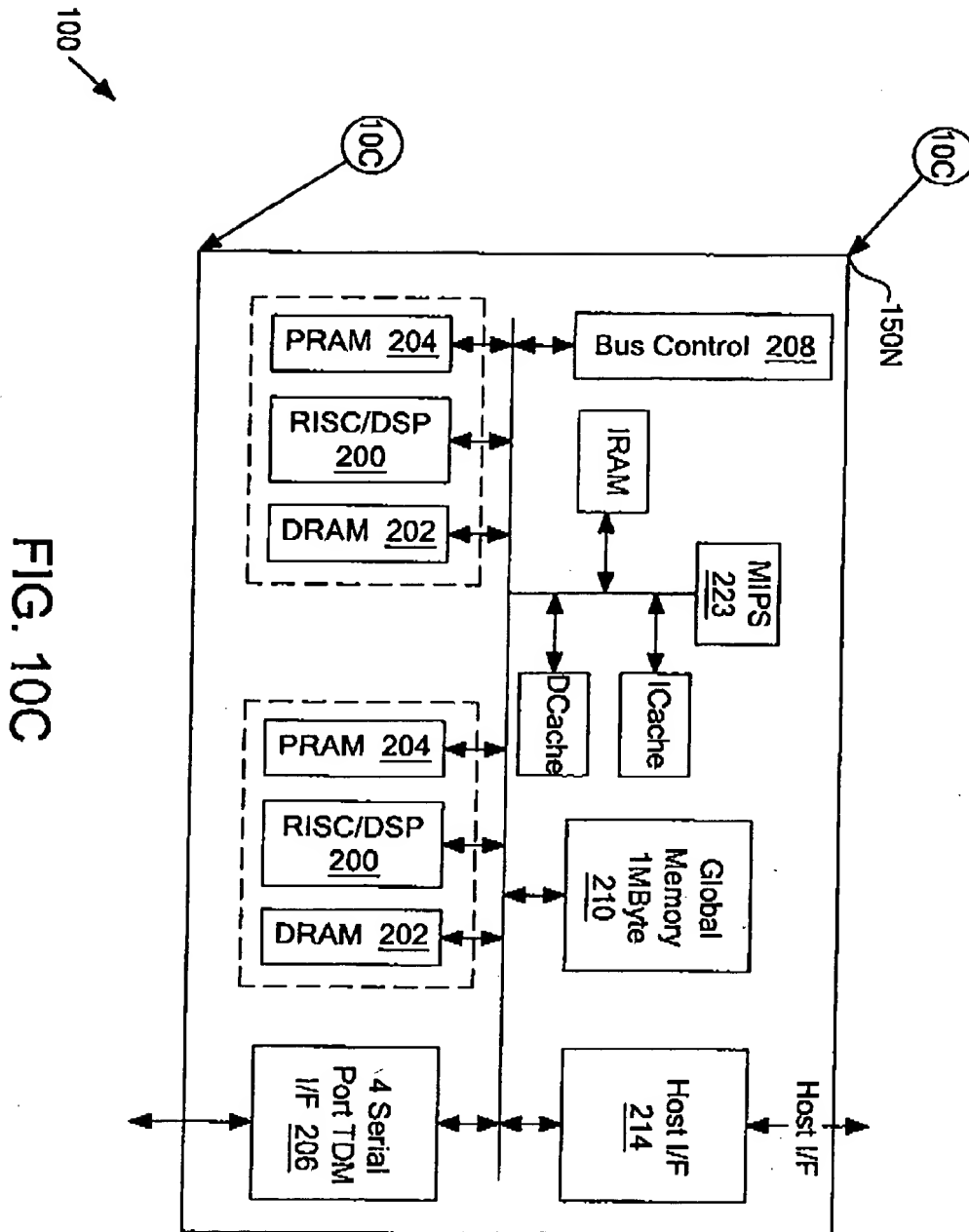
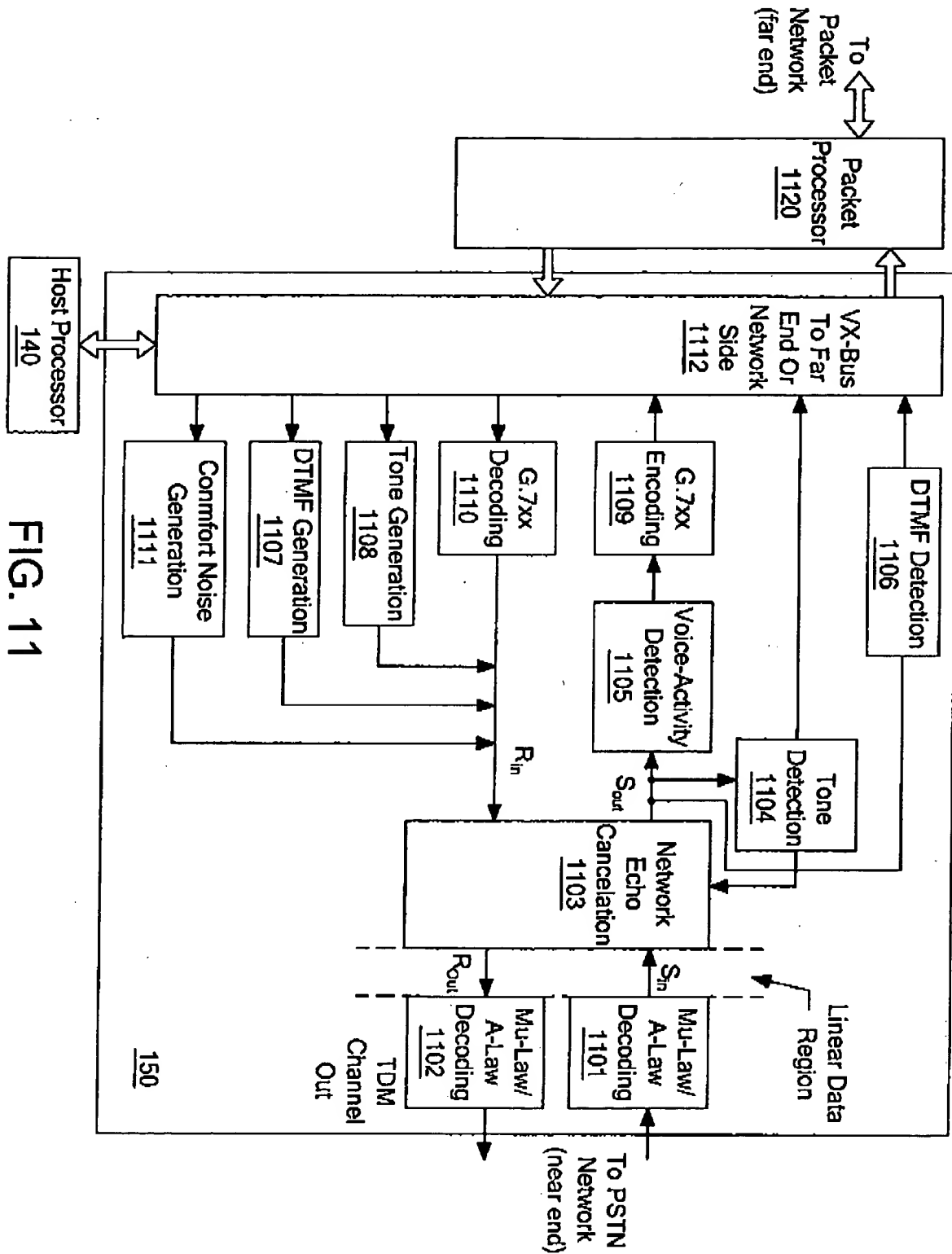


FIG. 10B

Replacement Sheet 09/938 104



Replacement Sheet 09/938 10f



Replacement Sheet 09/938 104

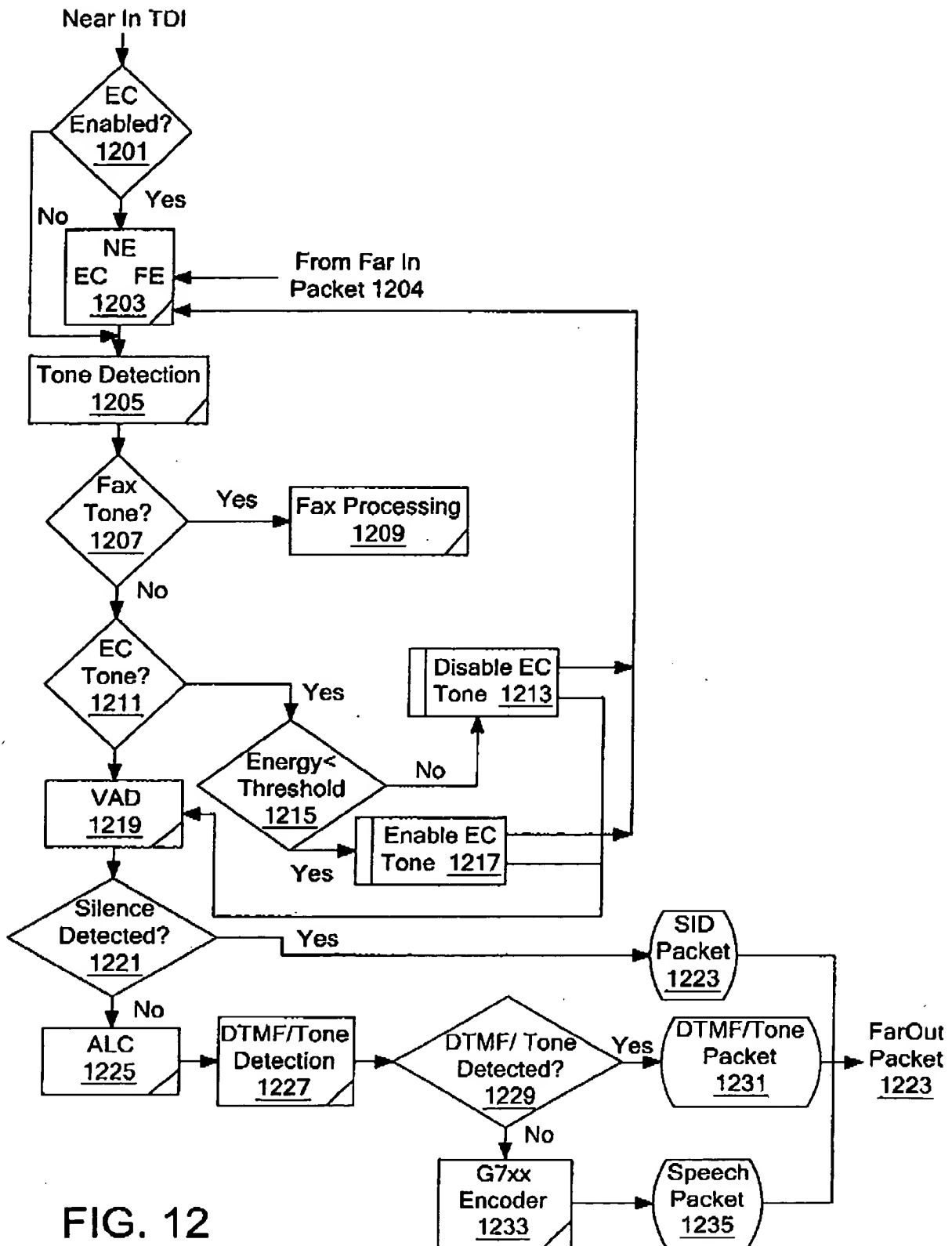


FIG. 12

Replacement Sheet 09/938104

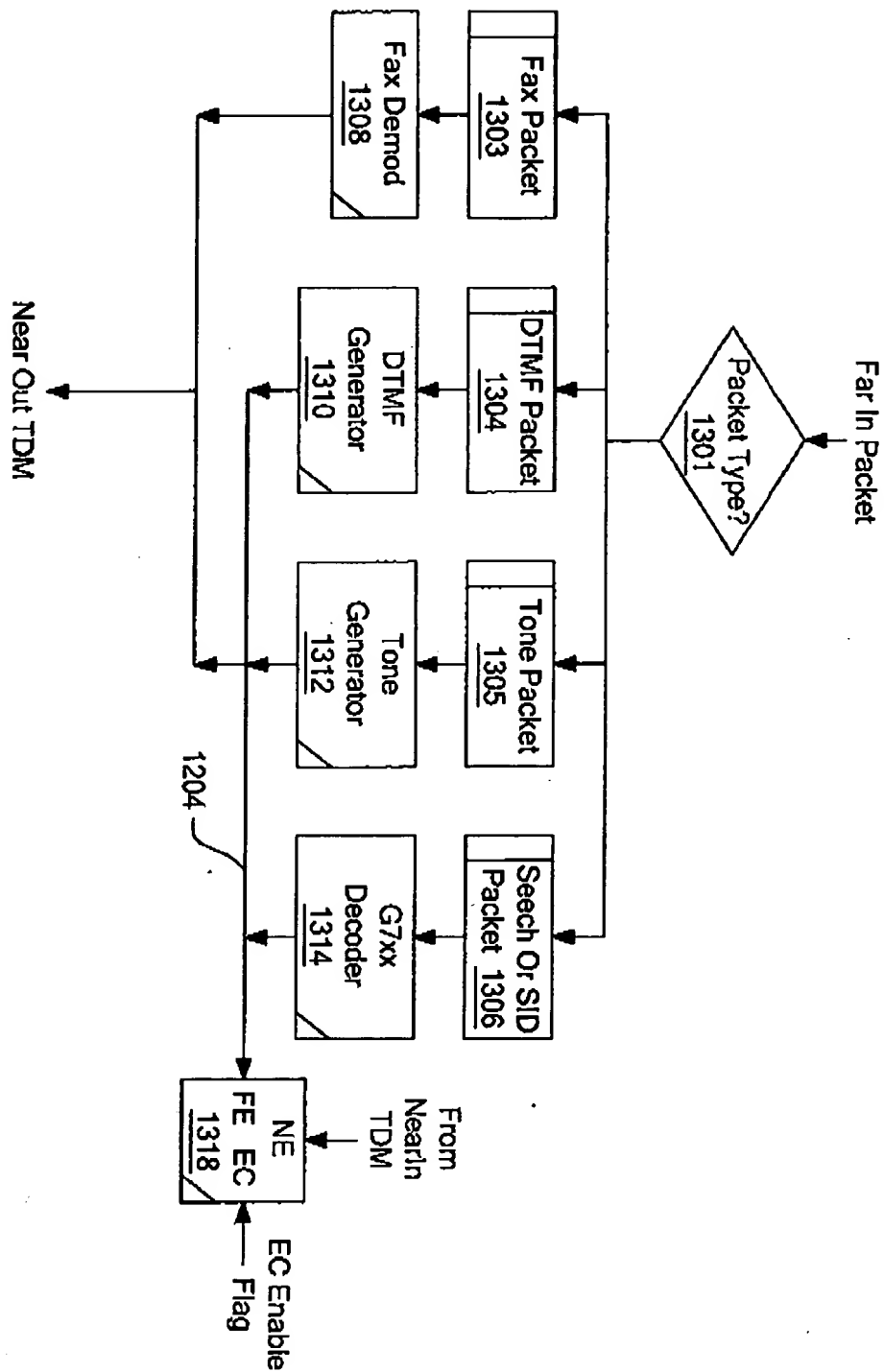
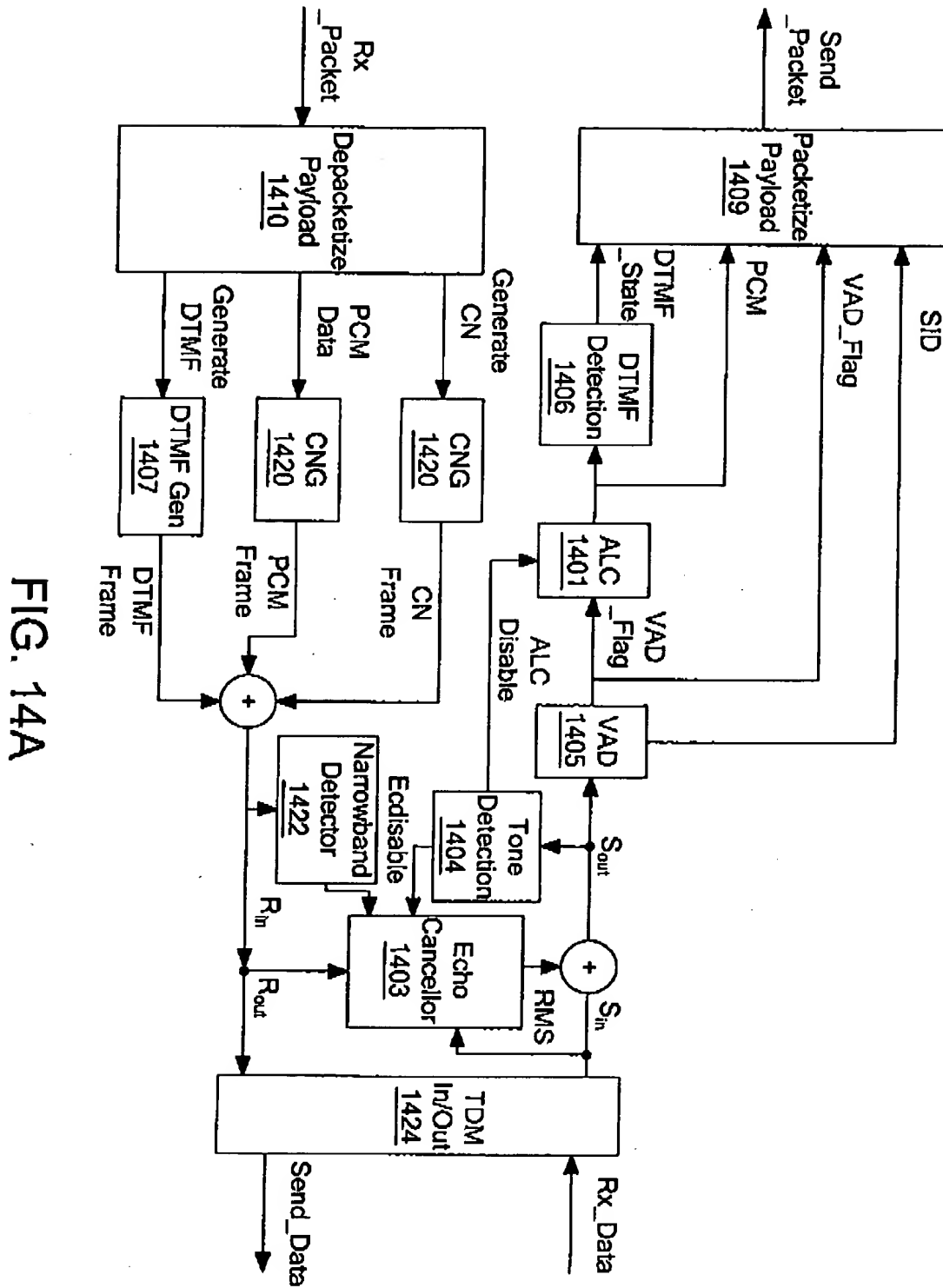


FIG. 13

Replacement Sheet 09/938 104



Replacement Sheet 09/938 104

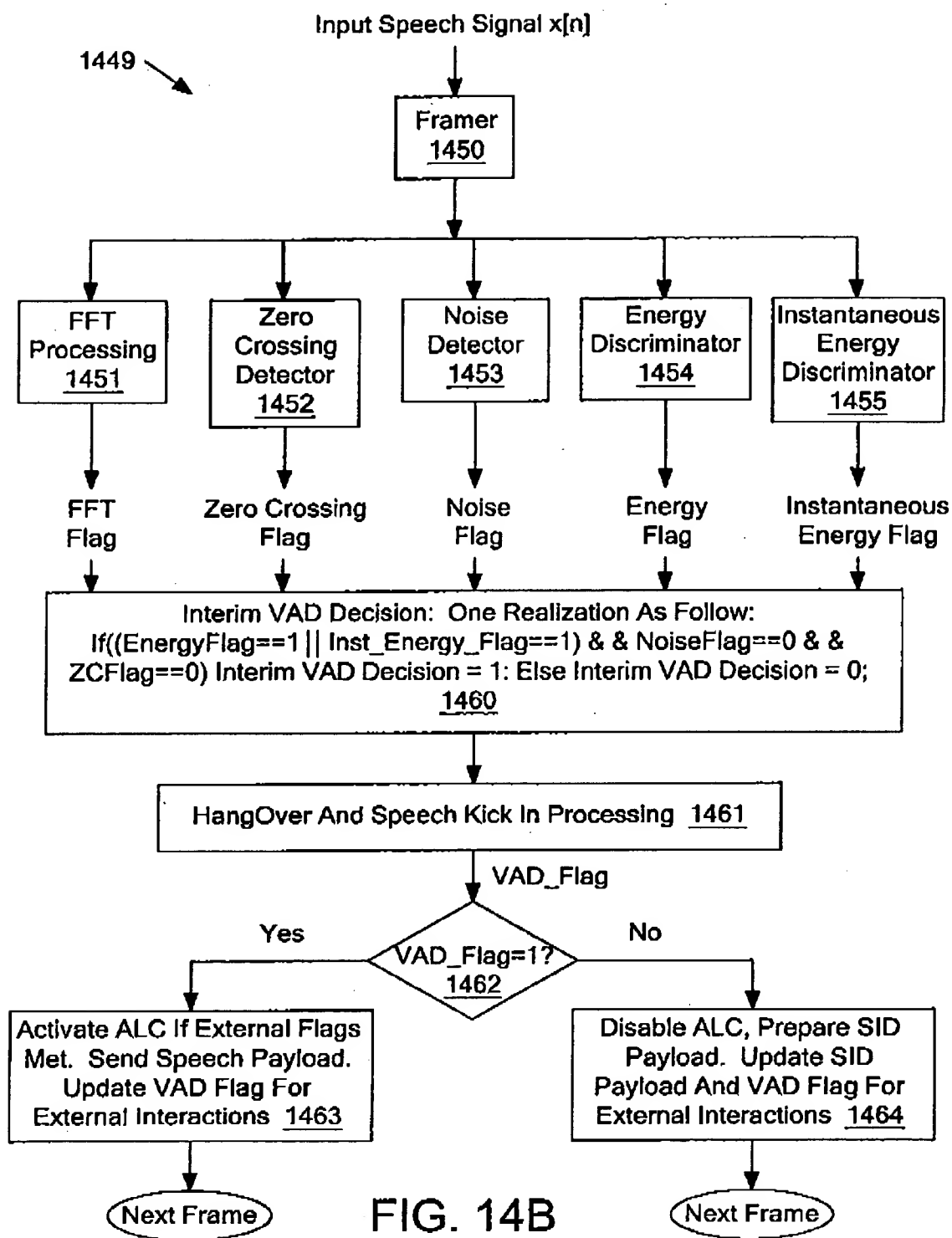
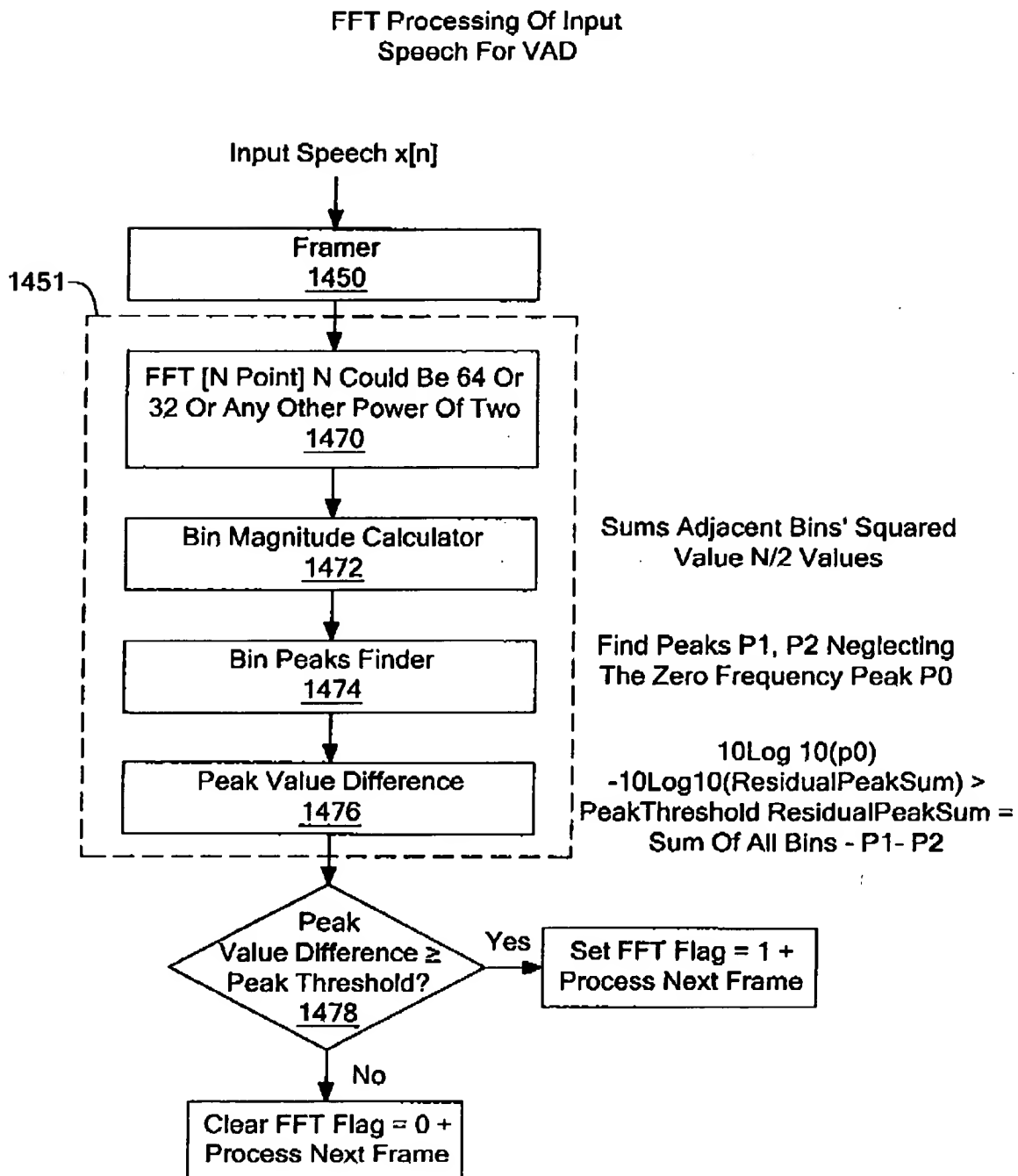
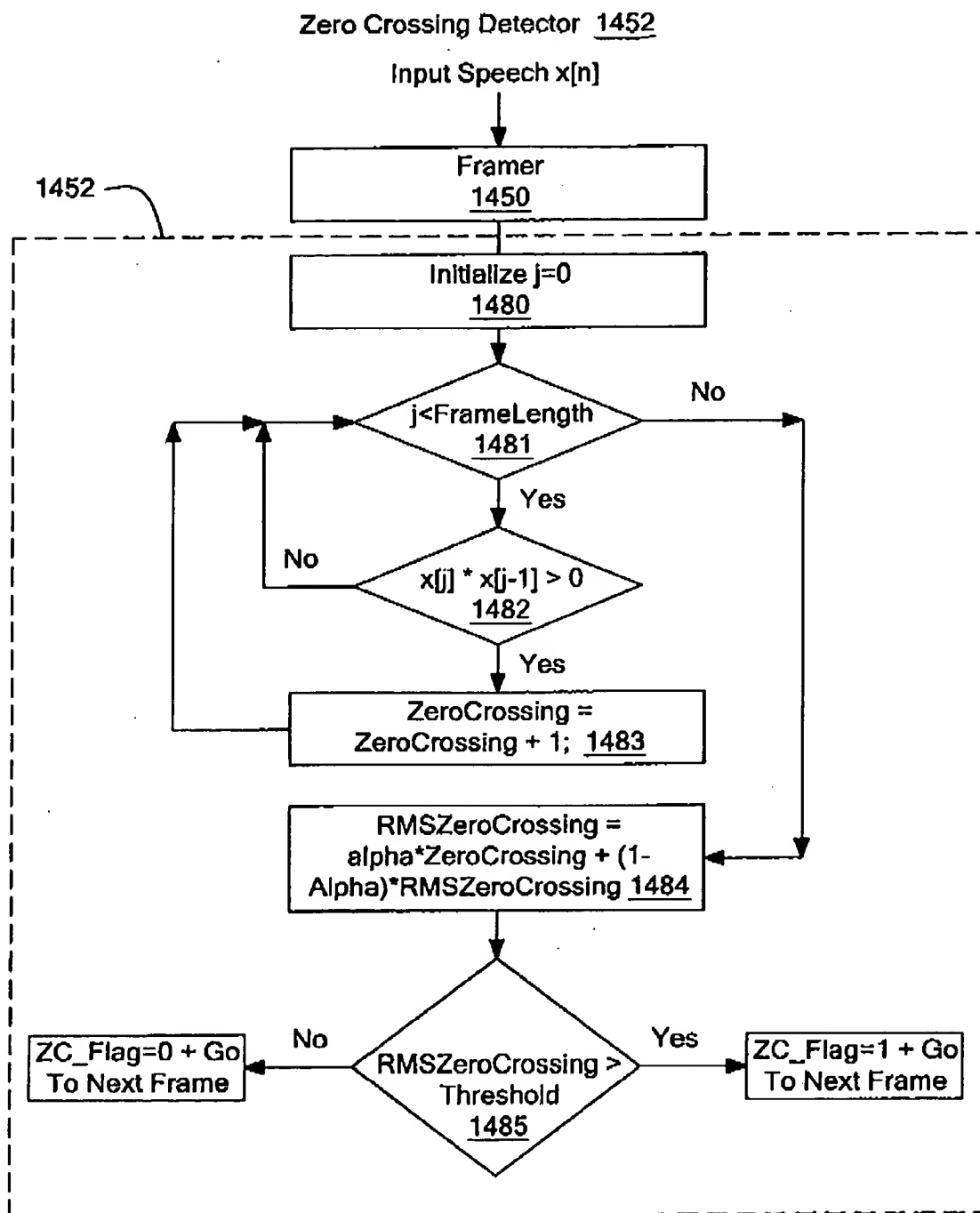


FIG. 14B

Replacement Sheet 09/938104



Replacement Sheet 09/938104



Replacement Sheet 09/938 104

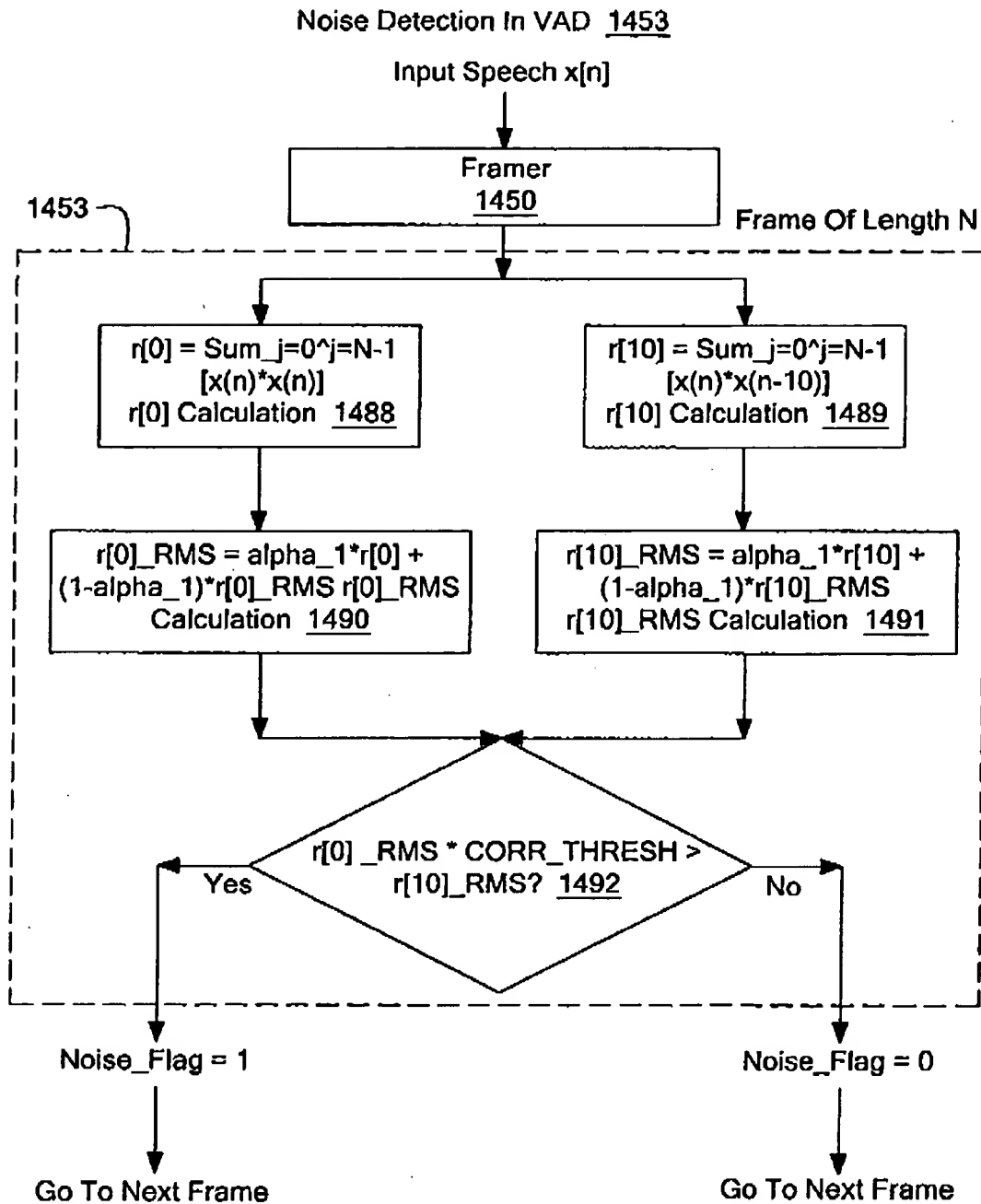


FIG. 14E

Replacement Sheet 09/938 104

## Energy Discriminator 1454

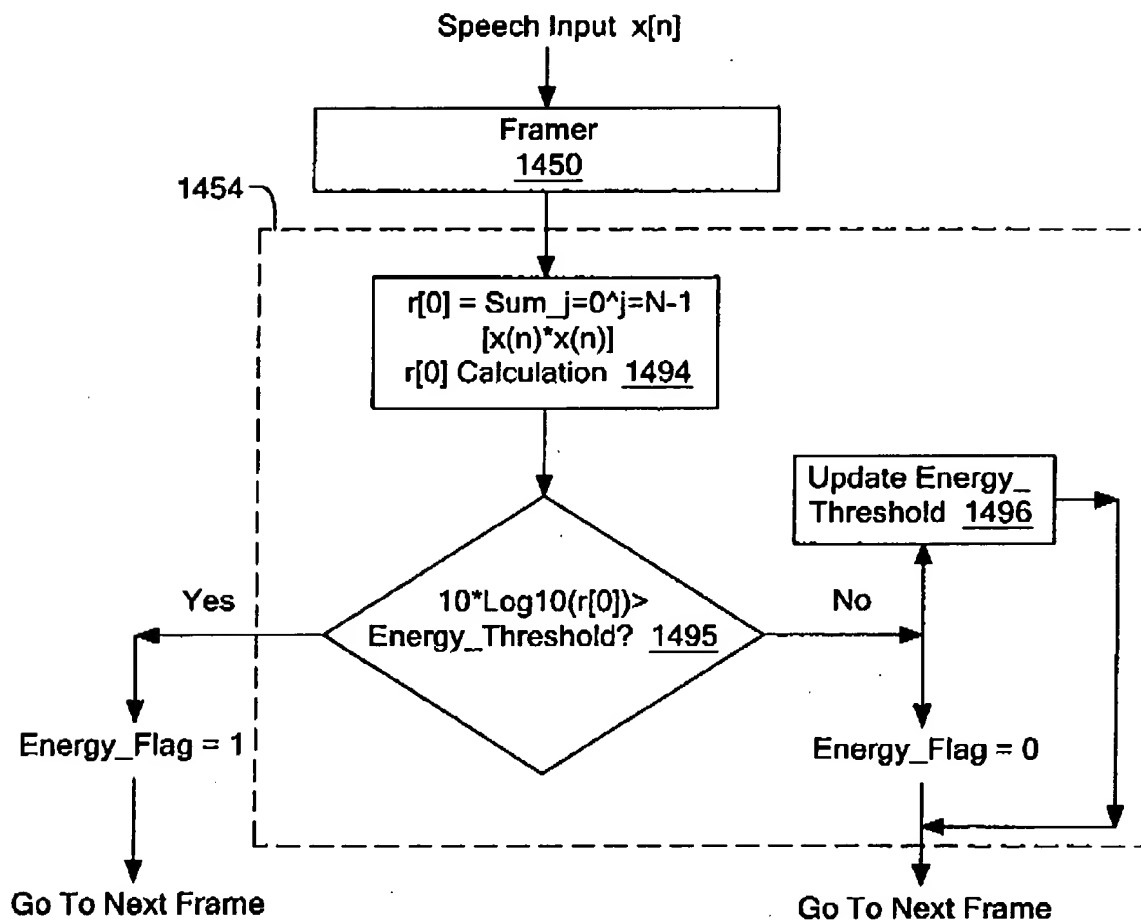


FIG. 14F

Replacement Sheet 09/938104

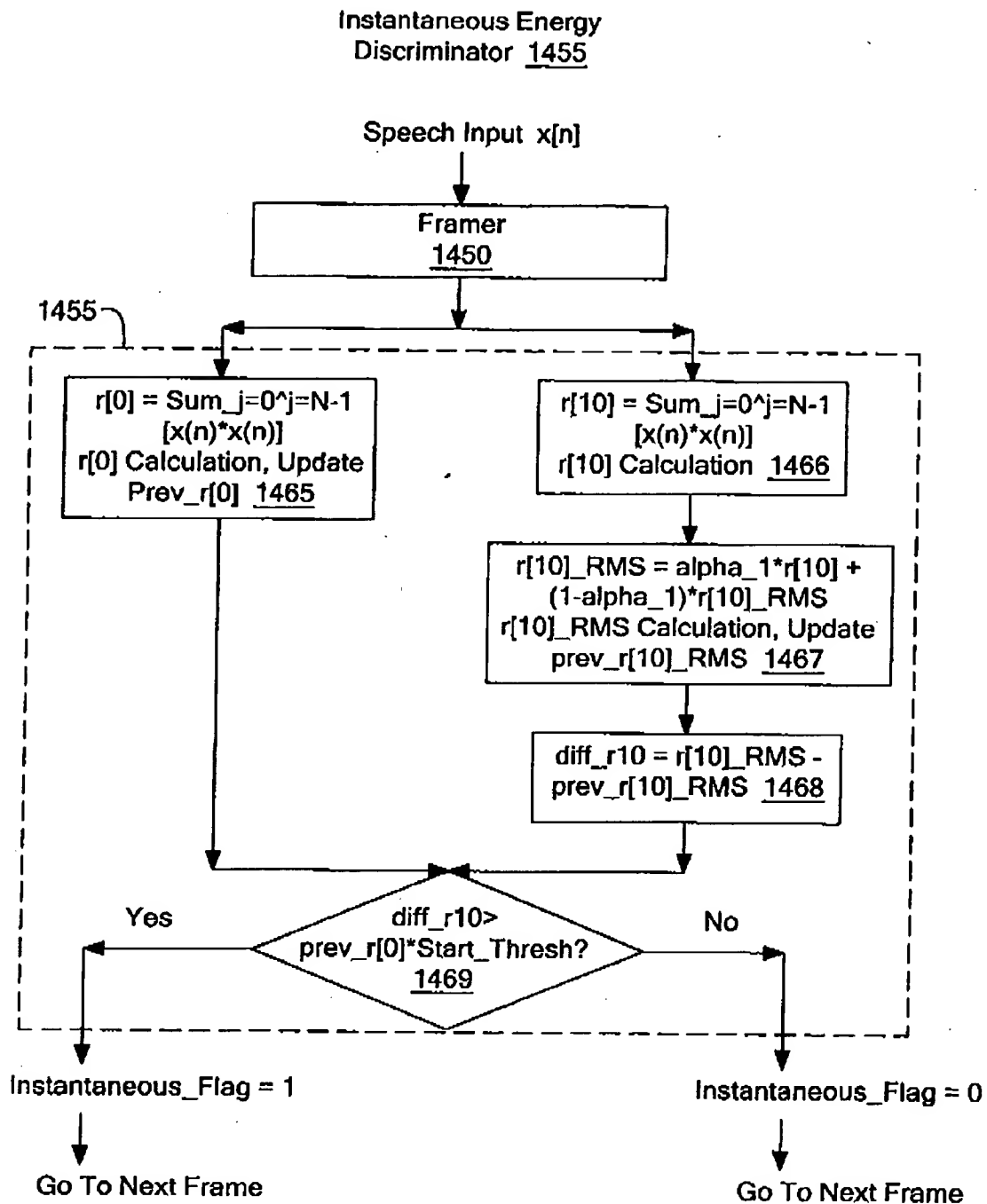


FIG. 14G

Replacement Sheet 09/938104

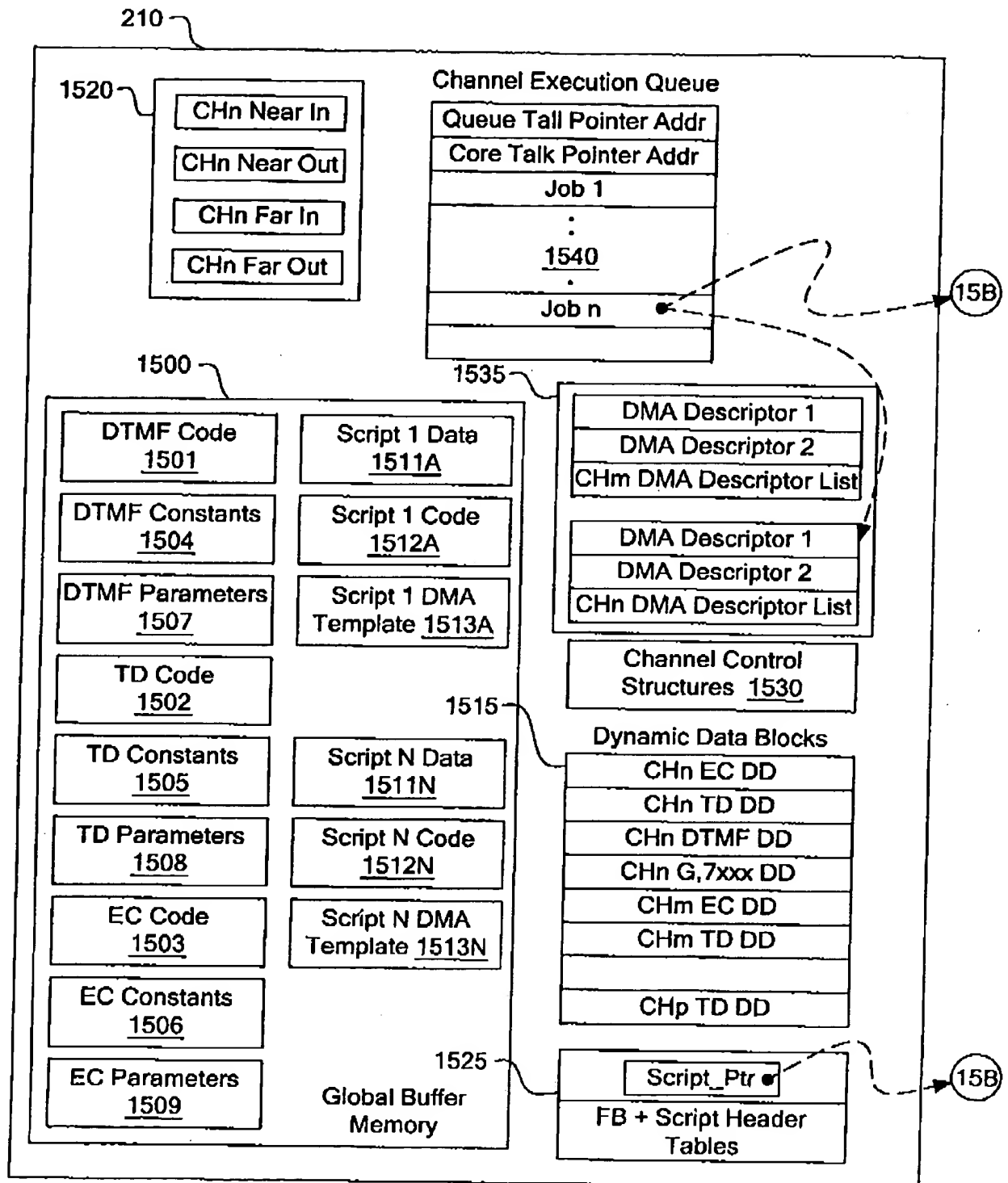


FIG. 15A

Replacement Sheet 09/938 104

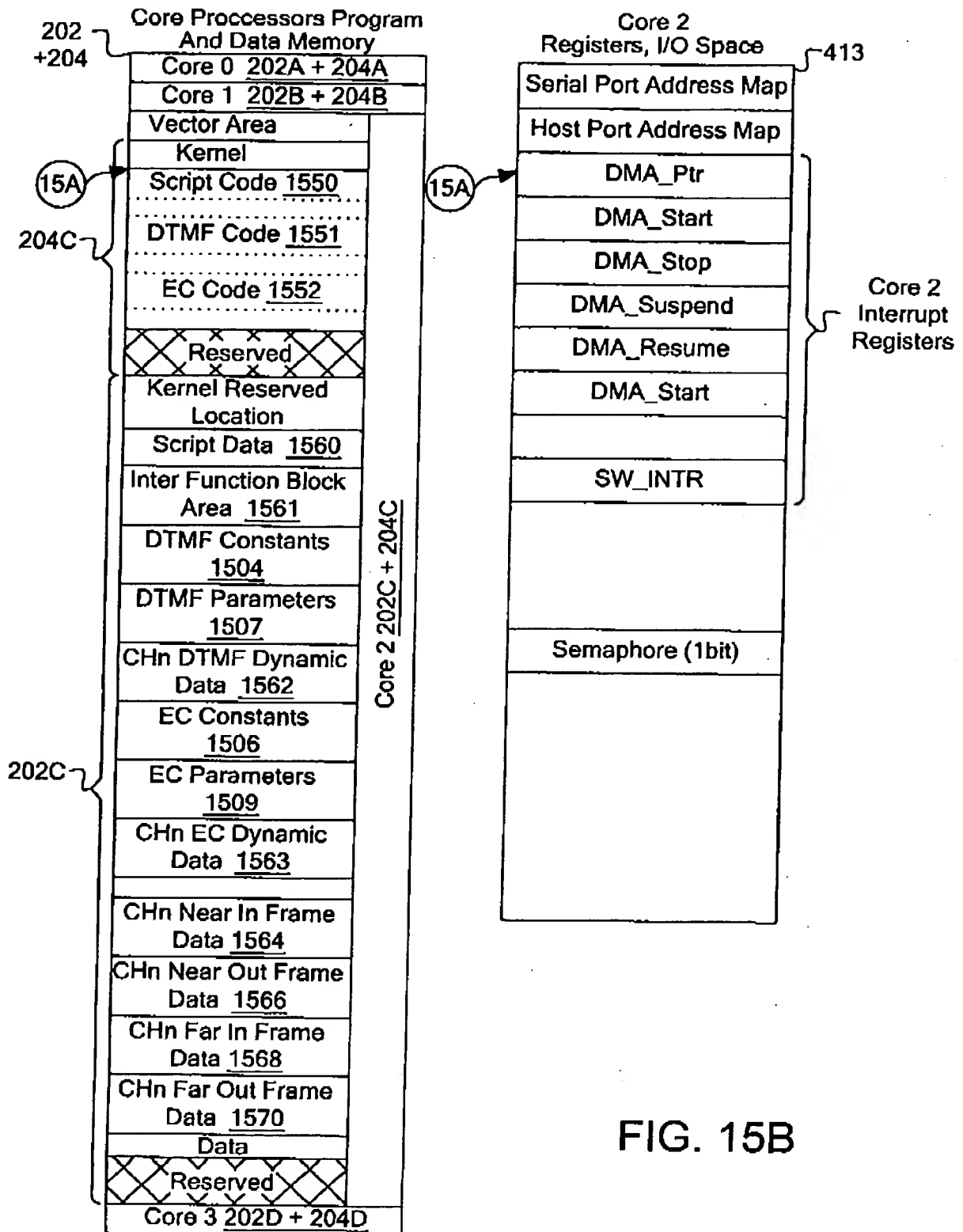


FIG. 15B

Replacement Sheet 09/938104

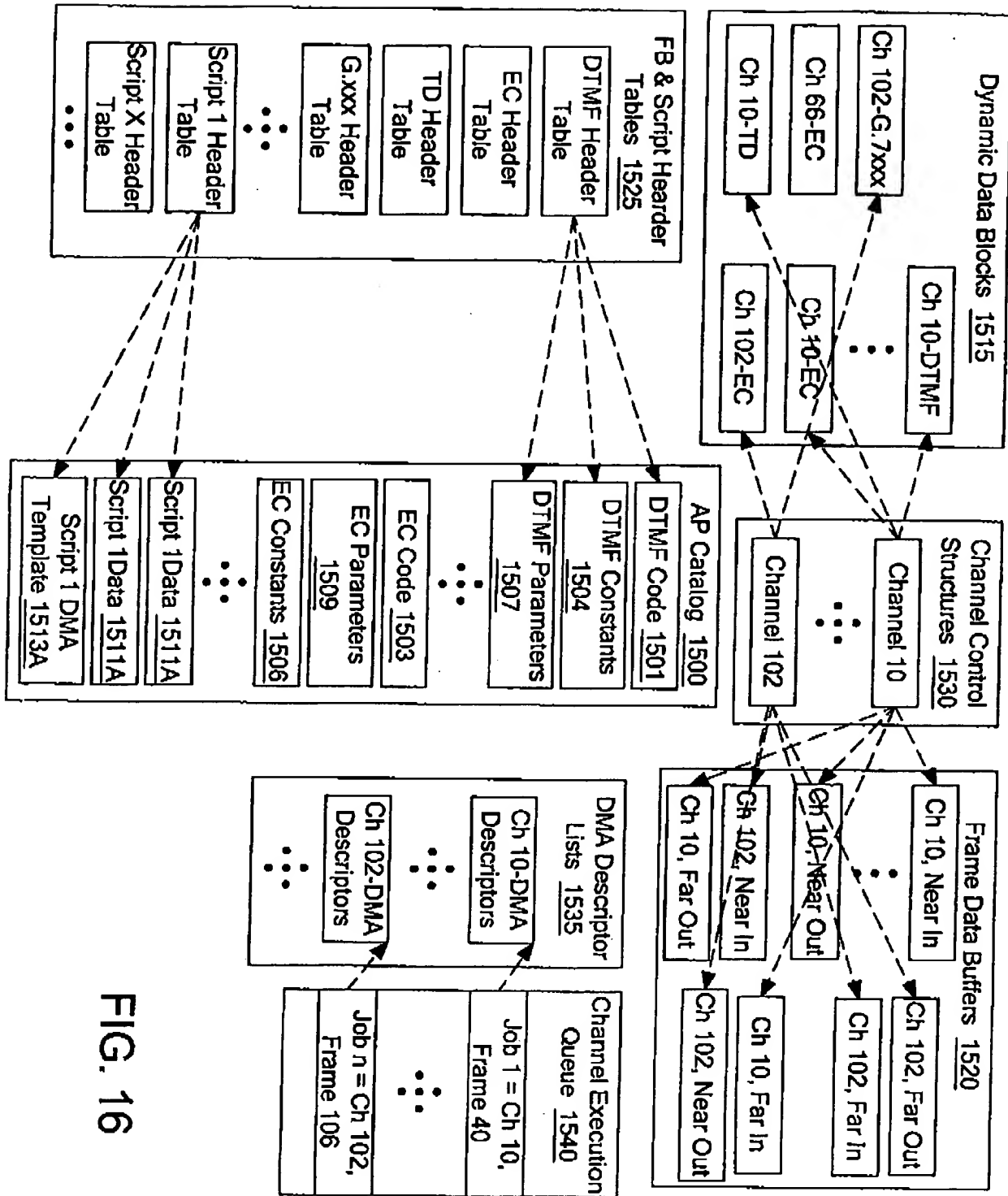


FIG. 16

Replacement Sheet 09/938604

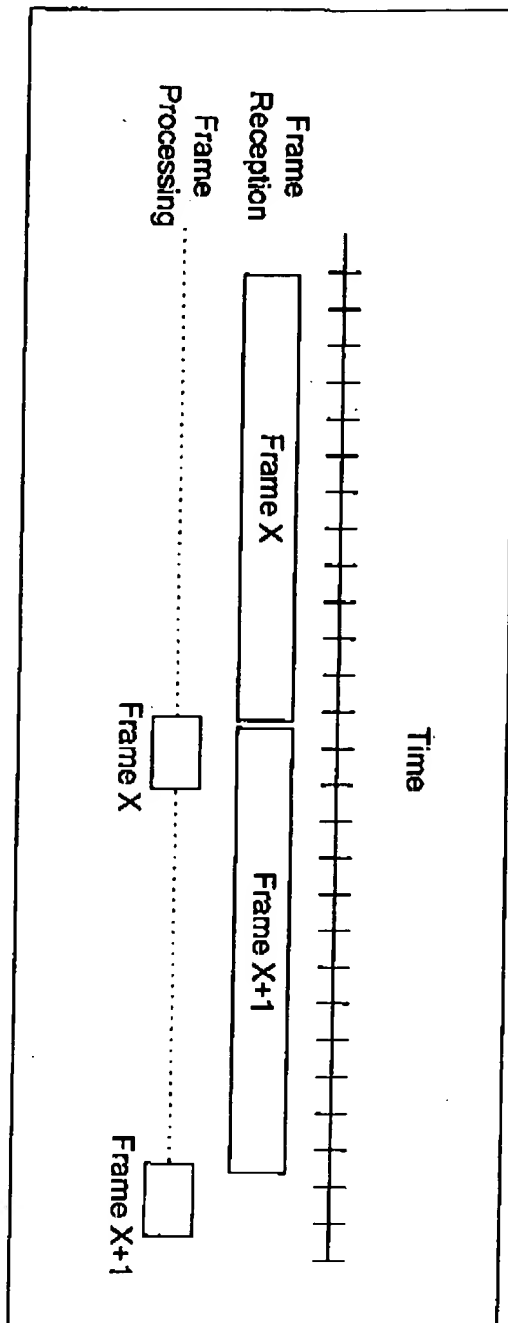


FIG. 17

Replacement Sheet 09/938104

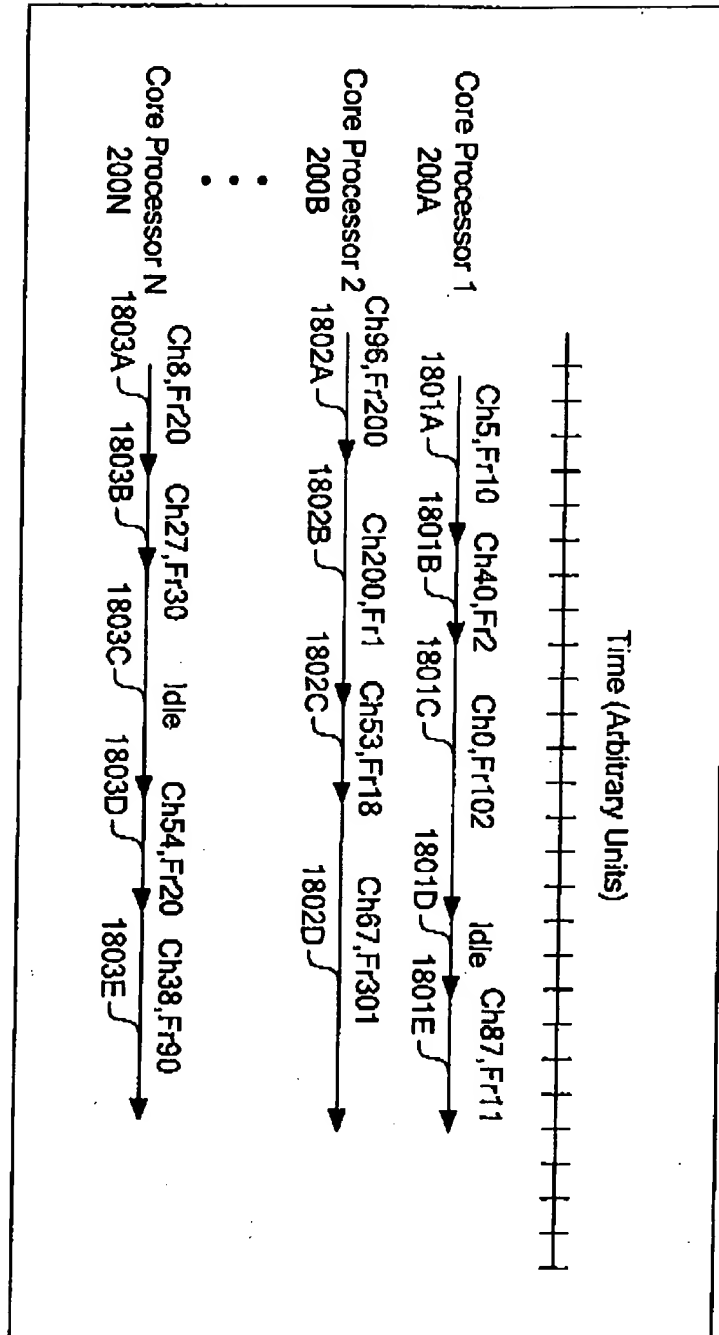


FIG. 18